

PRODUCT OVERVIEW

NSi83085 is a high reliability isolated half duplex RS-485 transceiver based on Novosense digital isolation technology, while NSi83086 is an isolated full duplex RS-485 transceiver. Both devices are safety certified by UL1577 support 5kV_{RMS} insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption.

The Bus pins of NSi83085/NSi83086 are protected from ±16kV system level ESD to GND₂ on Bus side. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

The data rate of NSi83085 is 500kbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line. The data rate of NSi83086 is up to 16Mbps.

Key Features

- Up to 5000V_{RMS} Insulation voltage
- Bus side power supply voltage: 3.0V to 5.5V
- VDD₁ supply voltage: 2.5V to 5.5V
- High CMTI : ±150kV/us
- High system level EMC performance:
 - Bus Pins meet IEC61000-4-2 ±16kV ESD
 - Other Pins meet ±7kV contact ESD
- Fail-safe protection receiver
- NSi83085 has slew rate limitation
- Up to 256 transceivers on the bus
- Isolation Barrier Life: >60 years
- Operation temperature: -40°C~85°C

- RoHS-compliant packages:
SOIC-16 wide body

Safety Regulatory Approvals (pending)

- UL recognition: up to 5000V_{RMS} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-10 (VDE V 0884-10): 2006-12

Applications

- Industrial automation system
- Isolated RS-485 communication
- Smart electric meter and water meter
- Security and protection monitoring

Functional Block Diagrams

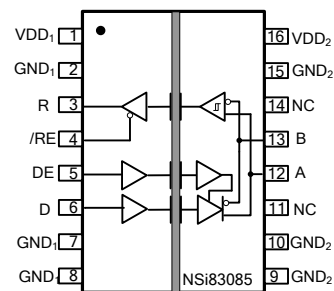


Figure 1. NSi83085 Block Diagram

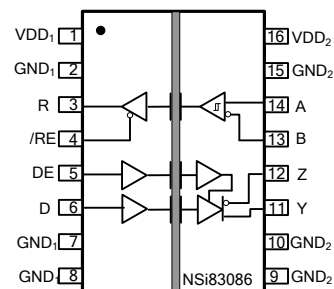


Figure 2. NSi83086 Block Diagram

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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD ₁ , VDD ₂	-0.5		6	V	
Maximum Input Voltage	/RE, DE, TxD	-0.4		VDD+0.4	V	
Common-Mode Transients	CMTI	-150		150	kV/us	
Driver Output/Receiver Input Voltage	VA, VB, VY, VZ	-7		12	V	
Receiver Output Current	I _o	-15		15	mA	
Maximum Surge Isolation Voltage	V _{IOSM}			5.3	kV	
Operating Temperature	Topr	-40		85	°C	
Storage Temperature	Tstg	-40		150	°C	
Electrostatic discharge	HBM (Bus pins and GND)			±8000	V	
	HBM(All pins)			±6000	V	
	CDM			±2000	V	

2.0 SPECIFICATIONS

2.1. DC ELECTRICAL CHARACTERISTICS

(VDD₁=2.5V~5.5V, VDD₂=4.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD₁ = 5V, VDD₂ = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage	VDD ₁	2.5		5.5	V	
	VDD ₂	3.0		5.5	V	Bus Side
Logic-side supply current	I _{DD1}		3.32	4.98	mA	VDD ₁ =5V, DE=high, /RE=D =low, no load
			3.26	4.89	mA	VDD ₁ =3V, DE=high, /RE=D =low, no load
Bus-side supply current	I _{DD2}		3.35	5.02	mA	VDD ₂ =5V, DE=high, /RE=D =low, no load (NSi83085)
			2.15	3.23	mA	VDD ₂ =5V, DE=high, /RE=D =low, no load (NSi83085)

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Thermal-Shutdown Threshold	T_{TS}		165		°C	
Thermal-Shutdown Hysteresis	T_{TSH}		15		°C	
Common Mode Transient Immunity	CMTI	±100		±150	kV/us	
Logic Side						
Input High Voltage	V_{IH}	2			V	DE, D, /RE
Input Low Voltage	V_{IL}			0.8	V	DE, D, /RE
Input Threshold	V_{IT}		1.6		V	Input Threshold at rising edge
	V_{IT_HYS}		0.4		V	Input Threshold Hysteresis
Input Pull up Current	I_{PU}			20	uA	DE,/RE
Input Pull down Current	I_{PD}	-10			uA	DI
Output Voltage High	V_{OH}	VDD ₁ -0.3			V	$I_{OH} = -4mA$
Output Voltage Low	V_{OL}			0.3	V	$I_{OL} = 4mA$
Output Short-Circuit Current	I_{OSR}			110	mA	$0 \leq V_R \leq VDD_1$
Three-State Output Current	I_{OZ}	-15			uA	$0 \leq V_R \leq VDD_1$, /RE = high
Input Capacitance	C_{IN}		2		pF	DE, D, /RE
Driver						
Differential Output Voltage	$ V_{OD} $			VDD ₂	V	No Load
		2.7		VDD ₂	V	See Figure 2.4.1 , $R_L=100 \Omega$ (RS-422)
		2.1		VDD ₂	V	See Figure 2.4.1 , $R_L=54 \Omega$ (RS-485)
Change in magnitude of the differential output voltage	$\Delta V_{OD} $			0.2	V	See Figure 2.4.1 , $R_L=100 \Omega$ or $R_L=54 \Omega$
Common-Mode Output Voltage	$ V_{OC} $		VDD ₂ /2	3	V	See Figure 2.4.1 , $R_L=100 \Omega$ or $R_L=54 \Omega$
Change in Magnitude of Common-Mode Voltage	$\Delta V_{OC} $			0.2	V	See Figure 2.4.1 , $R_L=100 \Omega$ or $R_L=54 \Omega$
Driver Short-Circuit Output Current	I_{OSD}			250	mA	$0 \leq V_{OUT} \leq +12V$
		-250			mA	$-7V \leq V_{OUT} \leq VDD_2$
Output Leakage Current (Y and Z) Full-Duplex	I_O			125	uA	DE=GND, VIN=12V
		-75			uA	DE=GND, VIN=-7V

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Receiver						
Input Current (A and B)	I_A, I_B			125	uA	DE=GND, VDD ₂ =GND or VDD ₂ , V _{IN} =12V
		-200			uA	DE=GND, VDD ₂ =GND or VDD ₂ , V _{IN} =-7V
Receiver Differential Threshold Voltage	V_{TH}	-200	-125	-50	mV	$-7V \leq V_{CM} \leq 12V$
Receiver Input Hysteresis	ΔV_{TH}		15		mV	$V_A + V_B = 0$
Receiver Input Resistance	R_{IN}	96k Ω				$-7V \leq V_{CM} \leq 12V$, DE=low

2.2. SWITCHING ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 85°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Driver (NSi83085)						
Maximum Data Rate	f_{MAX}	0.5			Mbps	
Driver Propagation Delay	t_{PLH}		450	675	ns	See Figure 2.4.2, $R_L=54 \Omega$, $C_L=50pF$
	t_{PHL}		430	645	ns	See Figure 2.4.2, $R_L=54 \Omega$, $C_L=50pF$
Driver Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	PWD		20		ns	See Figure 2.4.2, $R_L=54 \Omega$, $C_L=50pF$
Driver Output Falling Time or Rising time	t_F		590	885	ns	See Figure 2.4.2, $R_L=54 \Omega$, $C_L=50pF$
	t_R		590	885	ns	See Figure 2.4.2, $R_L=54 \Omega$, $C_L=50pF$
Driver Enable to Output High	t_{ZH}		310	465	ns	See Figure 2.4.3, $R_L=110 \Omega$, $C_L=50pF$
Driver Enable to Output Low	t_{ZL}		310	465	ns	See Figure 2.4.3, $R_L=110 \Omega$, $C_L=50pF$
Driver Output High to Disable	t_{HZ}		30	45	ns	See Figure 2.4.3, $R_L=110 \Omega$, $C_L=50pF$
Driver Output Low to Disable	t_{LZ}		30	45	ns	See Figure 2.4.3, $R_L=110 \Omega$, $C_L=50pF$
Receiver (NSi83085)						
Maximum Data Rate	f_{MAX}	0.5			Mbps	
Receiver Propagation Delay	t_{PLH}		102	153	ns	See Figure 2.4.4,

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						C_L=15pF
	t _{PHL}		92	138	ns	See Figure 2.4.4, C_L=15pF
Receiver Pulse Width Distortion	PWD		10		ns	 t_{PHL} - t_{PLH} , See Figure 2.4.4, C_L=15pF
Receiver Output Falling Time or Rising time	t _F		2.5	3.75	ns	See Figure 2.4.4, C_L=15pF
	t _R		2.5	3.75	ns	See Figure 2.4.4, C_L=15pF
Receiver Enable to Output High	t _{ZH}		18.5	27.75	ns	See Figure 2.4.5, R_L=1kΩ, C_L=15pF
Receiver Enable to Output Low	t _{ZL}		18.5	27.75	ns	See Figure 2.4.5, R_L=1kΩ, C_L=15pF
Receiver Disable to Output High	t _{HZ}		23	34.5	ns	See Figure 2.4.5, R_L=1kΩ, C_L=15pF
Receiver Disable to Output Low	t _{LZ}		23	34.5	ns	See Figure 2.4.5, R_L=1kΩ, C_L=15pF
Driver (NSi83086)						
Maximum Data Rate	f _{MAX}	16			Mbps	
Driver Propagation Delay	t _{PLH}		12	18	ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
	t _{PHL}		13.5	20.25	ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
Driver Pulse Width Distortion, t _{PHL} - t _{PLH}	PWD		1.5		ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
Driver Output Falling Time or Rising time	t _F		2.95	4.425	ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
	t _R		2.6	3.9	ns	See Figure 2.4.2, R_L=54Ω, C_L=50pF
Driver Enable to Output High	t _{ZH}		18.5	27.75	ns	See Figure 2.4.3, R_L=110Ω, C_L=50pF
Driver Enable to Output Low	t _{ZL}		19.1	28.65	ns	See Figure 2.4.3, R_L=110Ω, C_L=50pF
Driver Disable to Output High	t _{HZ}		20.8	31.2	ns	See Figure 2.4.3, R_L=110Ω, C_L=50pF
Driver Disable to Output Low	t _{LZ}		20.1	30.15	ns	See Figure 2.4.3, R_L=110Ω, C_L=50pF
Receiver (NSi83086)						
Maximum Data Rate	f _{MAX}	16			Mbps	

Receiver Propagation Delay	t_{PLH}		16.2	24.3	ns	See Figure 2.4.4, $C_L=15pF$
	t_{PHL}		22.2	33.3	ns	See Figure 2.4.4, $C_L=15pF$
Receiver Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	PWD		6.0		ns	See Figure 2.4.4, $C_L=15pF$
Receiver Output Falling Time or Rising time	t_F		2.3	3.45	ns	See Figure 2.4.4, $C_L=15pF$
	t_R		2.1	3.15	ns	See Figure 2.4.4, $C_L=15pF$
Receiver Enable to Output High	t_{ZH}		13.8	20.7	ns	See Figure 2.4.5, $R_L=1k\Omega, C_L=15pF$
Receiver Enable to Output Low	t_{ZL}		12.6	18.9	ns	See Figure 2.4.5, $R_L=1k\Omega, C_L=15pF$
Receiver Disable to Output High	t_{HZ}		14	21	ns	See Figure 2.4.5, $R_L=1k\Omega, C_L=15pF$
Receiver Disable to Output Low	t_{LZ}		13.4	20.1	ns	See Figure 2.4.5, $R_L=1k\Omega, C_L=15pF$

2.3. TYPICAL PERFORMANCE CHARACTERISTICS

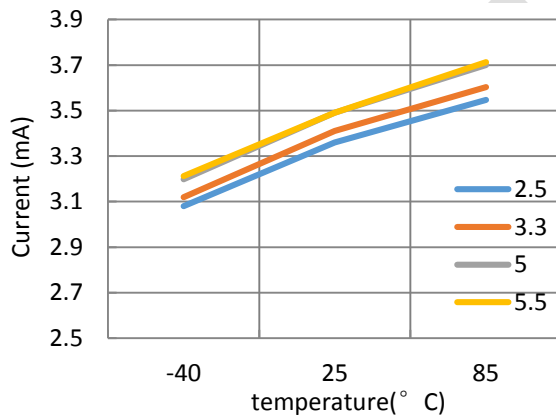


Figure 2.1 3085 VDD1 supply current vs Temperature

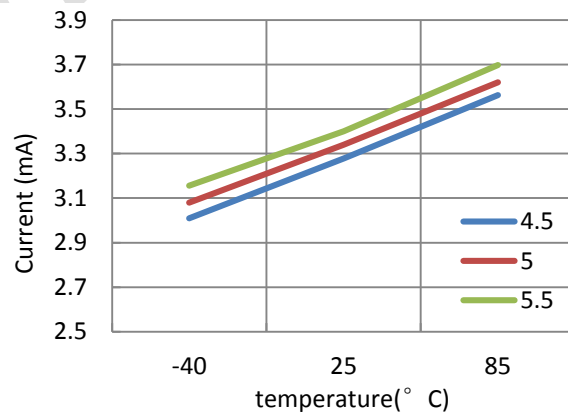


Figure 2.2 3085 VDD2 supply current vs Temperature

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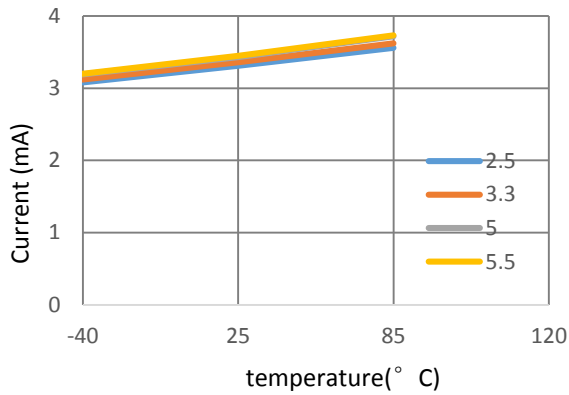


Figure 2.3 3086 VDD1 supply current vs Temperature

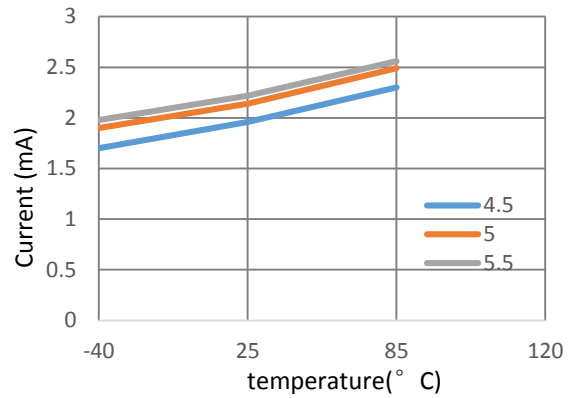


Figure 2.4 3086 VDD2 supply current vs Temperature

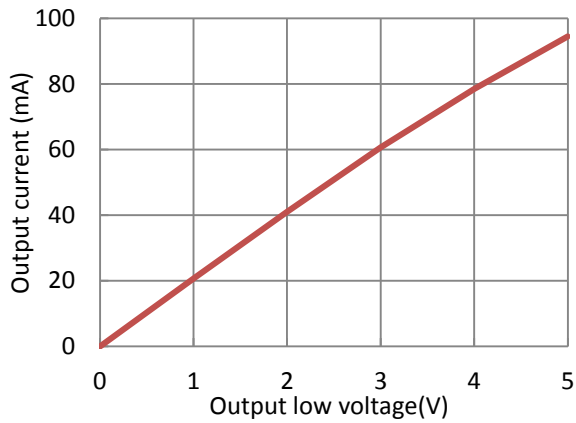


Figure 2.5 Receiver output current vs Output low voltage

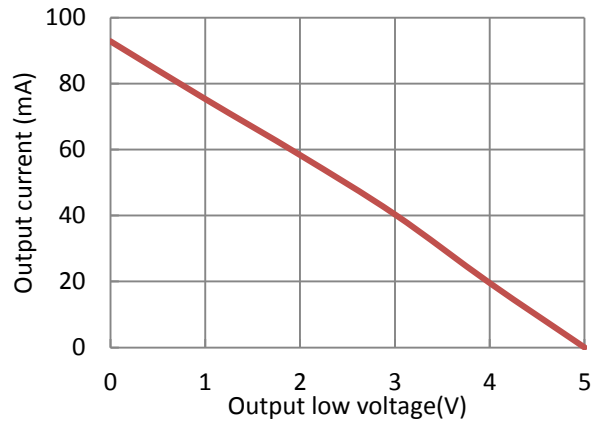


Figure 2.6 Receiver output current vs Output High voltage

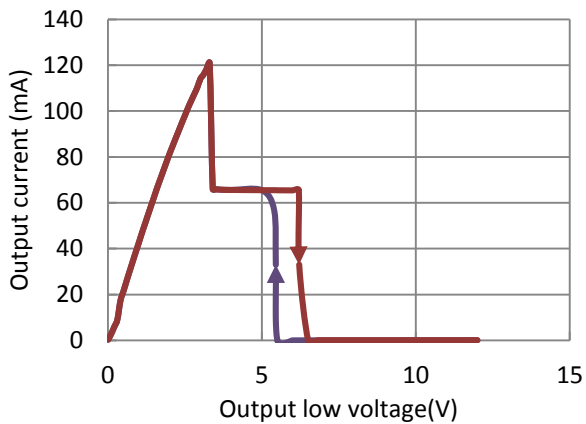


Figure 2.7 Driver output current vs Output Low voltage

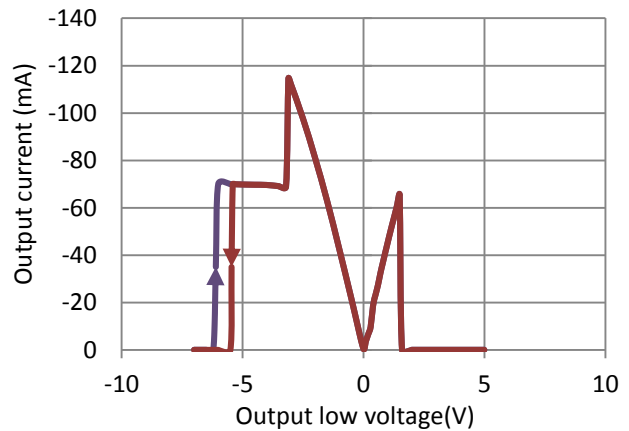


Figure 2.8 Driver output current vs Output High voltage

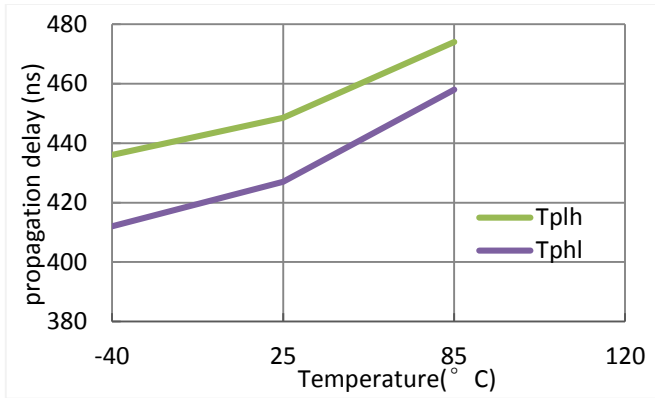


Figure 2.9 3085 Transmitter Propagation Delay vs Temperature

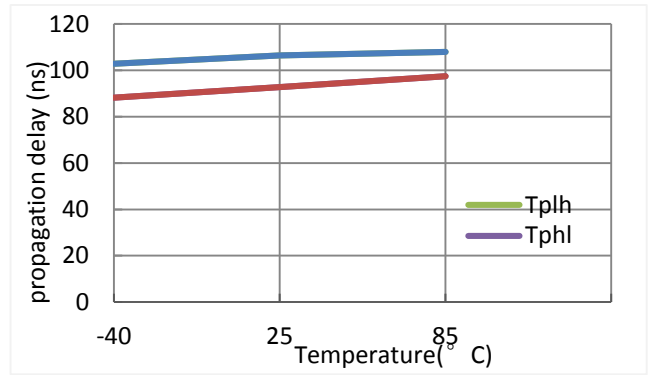


Figure 2.10 3085 Receiver Propagation Delay vs Temperature

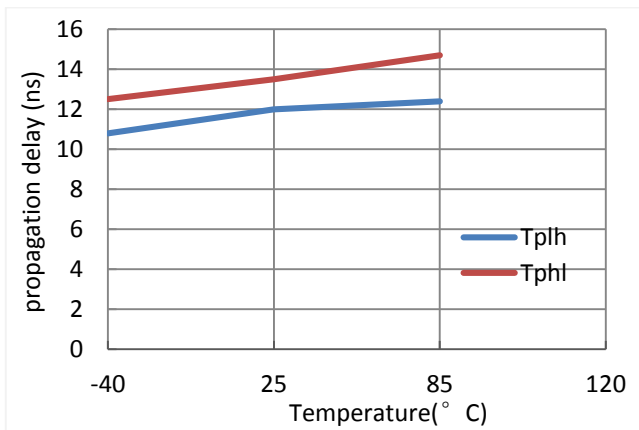


Figure 2.11 3086 Transmitter Propagation Delay vs Temperature

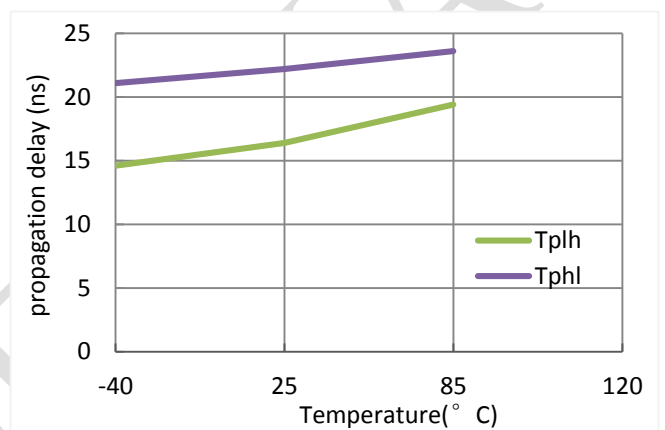


Figure 2.12 3086 Receiver Propagation Delay vs Temperature

2.4. PARAMETER MEASUREMENT INFORMATION

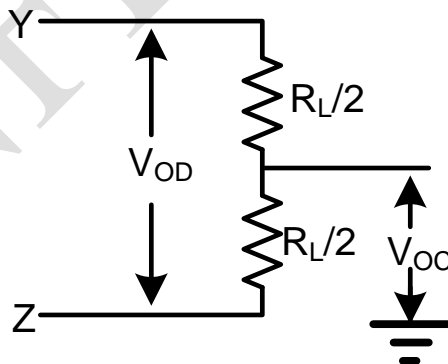


Figure 2.4.1 Driver DC Test Load

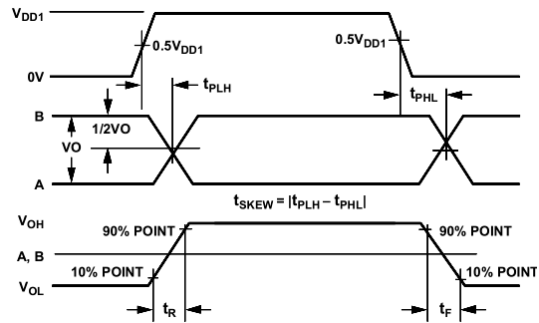
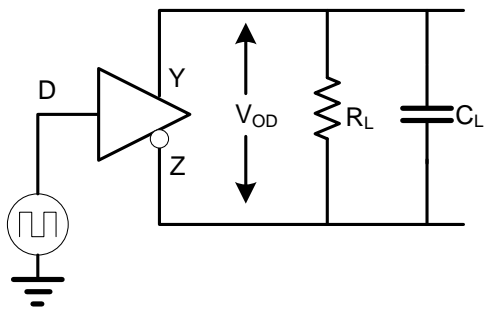


Figure 2.4.2 Driver Timing Test Circuit and waveform

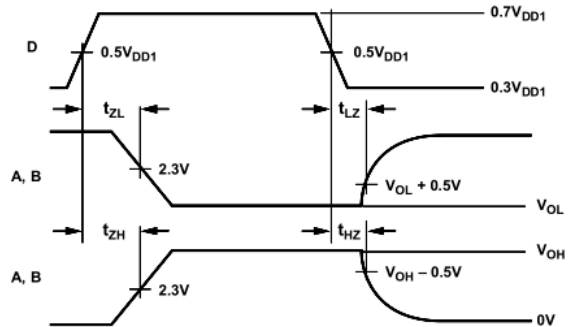
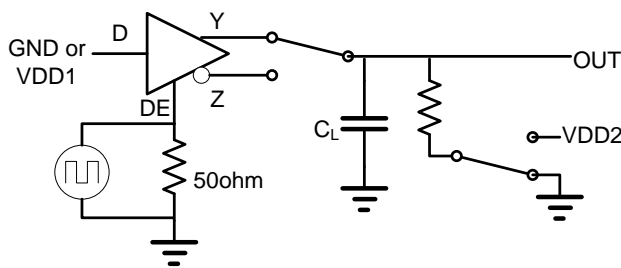


Figure 2.4.3 Driver Enable Disable Timing Test Circuit and waveform

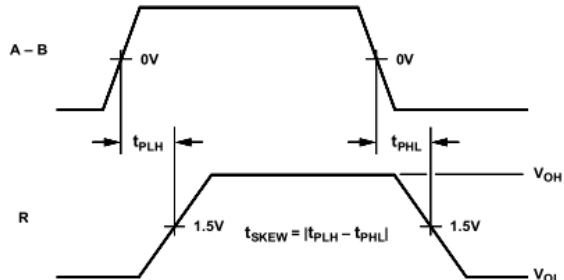
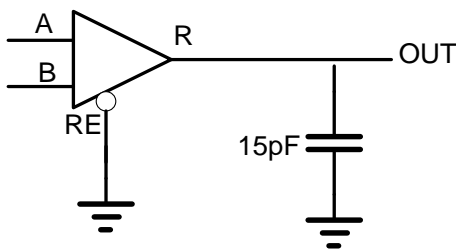


Figure 2.4.4 Receiver Propagation Delay Test Circuit and waveform

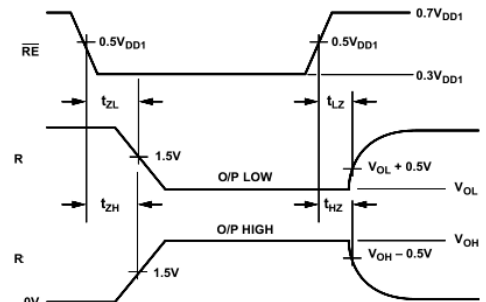
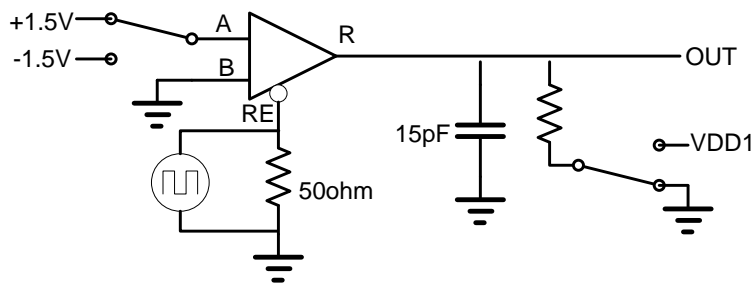


Figure 2.4.5 Receiver Enable Disable Timing Test Circuit and waveform

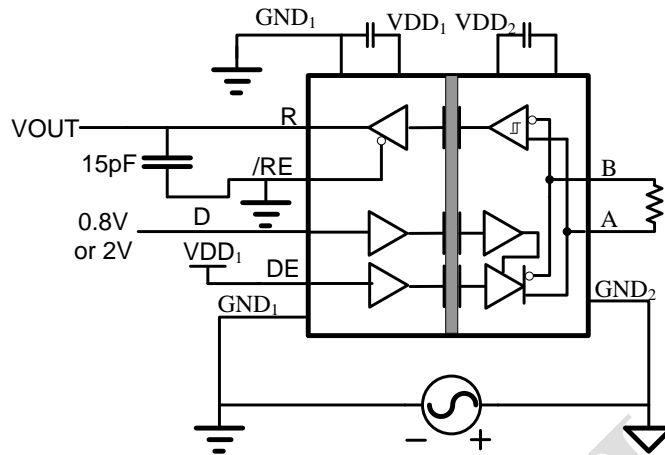


Figure 2.4.6 Common-Mode Transient Immunity Test Circuit

3.0 HIGH VOLTAGE FEATURE DESCRIPTION

3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	Symbol	Value	Unit	Comments
Minimum External Air Gap (Clearance)	L(I01)	7.8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	7.8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

3.2. DIN VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

Description	Test Condition	Symbol	Value	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	
For Rated Mains Voltage ≤ 400Vrms			I to IV	
Climatic Classification			10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	

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Maximum repetitive isolation voltage		V_{IORM}	800	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1200	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} =$ 60 sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	960	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} =$ 60 sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	960	Vpeak
Maximum transient isolation voltage	$t = 60$ sec	V_{IOTM}	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50us waveform, $V_{TEST} = 1.3 \times V_{IOSM}$	V_{IOSM}	5384	Vpeak
Isolation resistance	$V_{IO} = 500V$	R_{IO}	$> 10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.6	pF
Input capacitance		C_I	2	pF
Total Power Dissipation at 25°C		P_s	1499	mW
Safety input, output, or supply current	$\square \theta_{JA} = 140$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C	I_s		mA
	$\theta_{JA} = 84$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C		237	mA
Case Temperature		T_s	150	°C

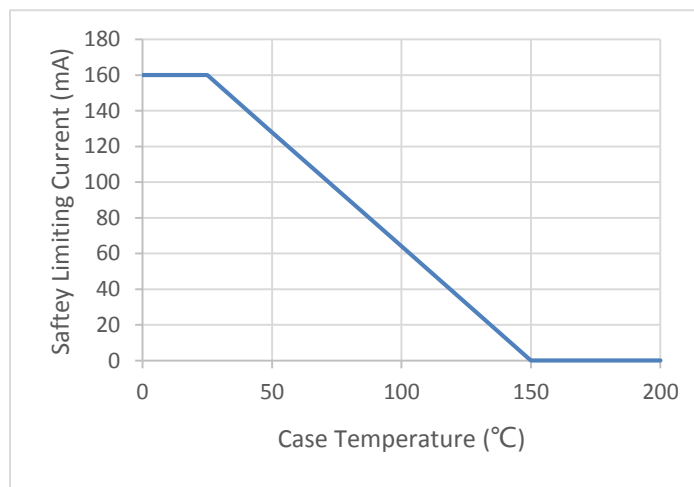


Figure 3.1 NSi83085/NSi83086 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

NSi83085/NSi83086

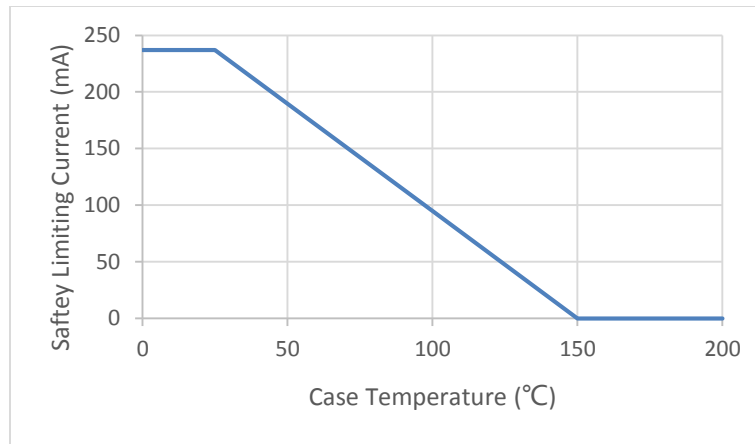


Figure 3.2 NSi83085/NSi83086 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

3.3. REGULATORY INFORMATION

The NSi83085/NSi83086 are approved or pending approval by the organizations listed in table.

UL	CSA	VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A IEC60950-1	DIN V VDE V0884-10 (VDE V 0884-10):2006-12	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000Vrms Isolation voltage	800V _{RMS} basic insulation working voltage 400V _{RMS} Reinforced insulation working voltage	Basic Insulation 1131Vpeak, V _{IOSM} =5384Vpeak	Basic insulation at 800V _{RMS} (1131Vpeak) Reinforced insulation at 400V _{RMS} (565Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

¹ In accordance with UL 1577, each NSi83085/NSi83086 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

² In accordance with DIN V VDE V 0884-10, each NSi8100W/NSi8101W is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

4.0 FUNCTION DESCRIPTION

NSi83085 is a high reliability isolated half duplex RS-485 transceiver, while NSi83086 is an isolated full duplex RS-485 transceiver. Data isolation is achieved using Novosense integrated capacitive isolation that allows data transmission between the logic side and the Bus side. Both devices are safety certified by UL1577 support 5kV_{RMS} insulation withstand voltages.

4.1. DATA RATE

The data rate of NSi83085 is 500kbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line. The data rate of NSi83086 is up to 16Mbps.

4.2. TRUE FAIL-SAFE RECEIVER INPUTS

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -50mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage ($V_A - V_B$) is greater than or equal to -50mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

4.3. TRUTH TABLES

Table 4.1 Driver Function Table

VDD1 status	VDD2 status	Input (D)	Enable Input (DE)	Outputs ¹	
				A/Y	B/Z
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Z	Z
PU	PU	X	OPEN	Z	Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Z	Z
PU	PD	X	X	Z	Z
PD	PD	X	X	Z	Z

¹PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance; Driver output pins are Y and Z for NSi83086, A and B for NSi83085;

Table 4.2 Receiver Function Table¹

VDD1 status	VDD2 status	Differential Input (V _A -V _B)	Enable Input (/RE)	Output
				(R)
PU	PU	≥-50mV	L/Open	H
PU	PU	≤-200mV	L/Open	L
PU	PU	Open/Short	L/Open	H
PU	PU	X	H	Z
PU	PU	Idle	L	H
PD	PU	X	X	Z
PU	PD	X	X	H
PD	PD	X	X	Z

¹PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.

4.4. THERMAL SHUTDOWN

The device is protected from over temperature damage by integrated thermal shutdown circuitry. When the junction temperature (T_J) exceeds +165°C (typ), the driver outputs go high-impedance. The device resumes normal operation when T_J falls below +145°C (typ).

5.0 APPLICATION NOTE

5.1. 256 TRANSCEIVERS ON THE BUS

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

5.2. ESD PROTECTION

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handing and assembly. The Bus pins have extra protection against static electricity to both the logic side (VDD1 side) and bus side (VDD2 side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- $\pm 8\text{kV}$ HBM.
- $\pm 16\text{kV}$ using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- $\pm 6\text{kV}$ HBM.
- $\pm 7\text{kV}$ using the Contact Discharge method specified in IEC 61000-4-2

5.3. LAYOUT CONSIDERATIONS

The NSi83085/NSi83086 requires a $0.1\ \mu\text{F}$ bypass capacitor between VDD1 and GND1, $10\ \mu\text{F}$ bypass capacitor between VDD2 and GND2. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to have the bus connectors and termination resistor as close as possible to the A and B, Y and Z pins.

5.4. TYPICAL APPLICATION

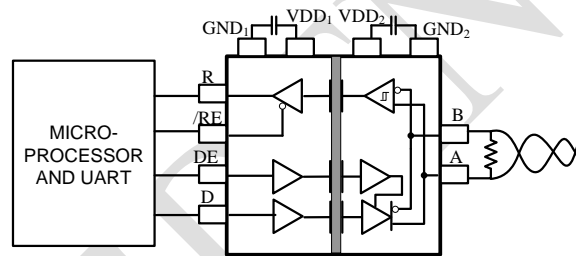


Figure 5.1 NSi83085 typical application circuit

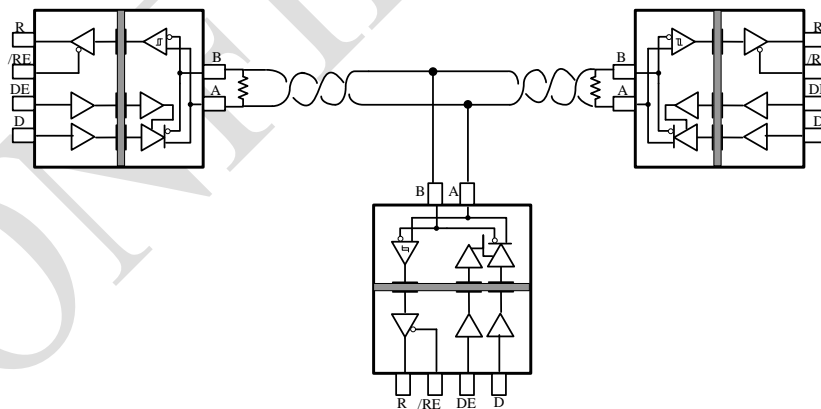


Figure 5.2 Typical isolated Half-Duplex RS-485 application

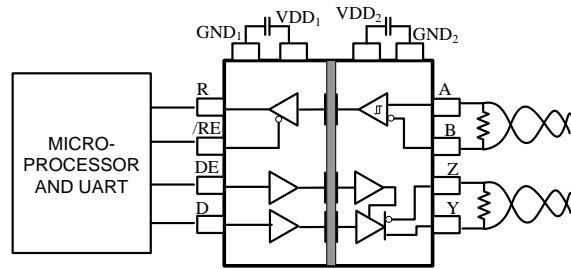


Figure 5.3 NSi83086 typical application circuit

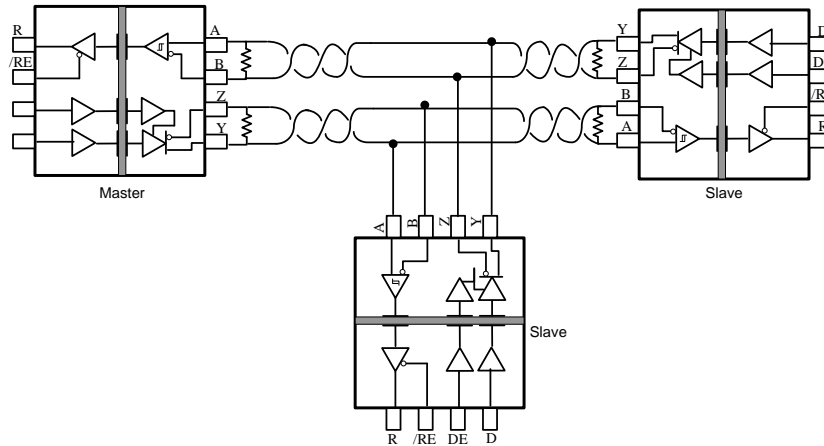


Figure 5.4 Typical isolated Full-Duplex RS-485 application

6.0 PACKAGE INFORMATION

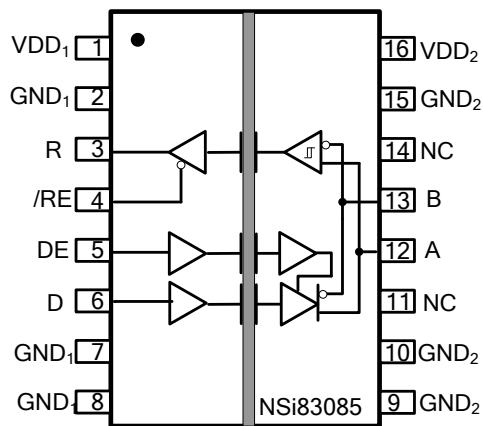


Figure 6.1 NSi83085 Package

NSi83085/NSi83086

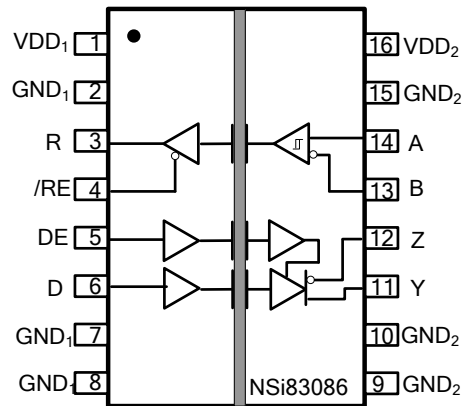


Figure 6.2 NSi83085 Package

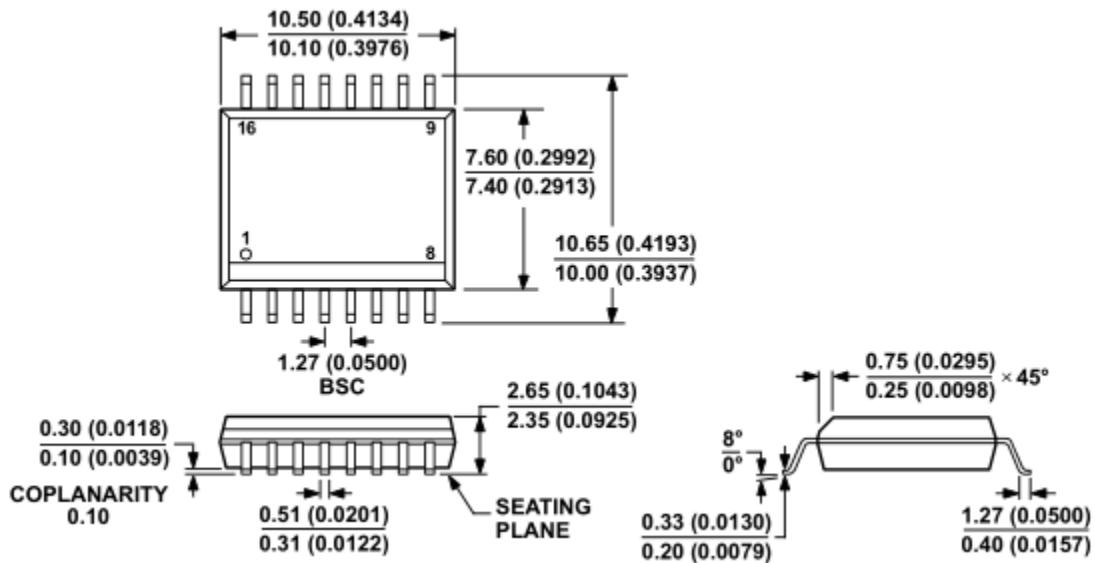


Figure 6.3 SOIC16 Package Shape and Dimension
Dimensions shown in millimeters and (inches)

Table 6.1 NSi83085 Pin Configuration and Description

NSi83085 PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Isolator Side 1
2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	R	Receive output
4	/RE	Receive enable input. This is an active low input.
5	DE	Driver enable input. This is an active high input
6	D	Driver transmit data input.
7	GND ₁	Ground 1, the ground reference for Isolator Side 1
8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	GND ₂	Ground 2, the ground reference for Isolator Side 2

NSi83085/NSi83086

10	GND ₂	Ground 2, the ground reference for Isolator Side 2
11	NC	No Connection.
12	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when VDD ₁ or VDD ₂ is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD ₁ or VDD ₂ is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
14	NC	No Connection.
15	GND ₂	Ground 2, the ground reference for Isolator Side 2
16	VDD ₂	Power Supply for Isolator Side 2

Table6.2 NSi83086 Pin Configuration and Description

<i>NSi83086</i> <i>PIN NO.</i>	<i>SYMBOL</i>	<i>FUNCTION</i>
1	VDD ₁	Power Supply for Isolator Side 1
2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	R	Receive output
4	/RE	Receive enable input. This is an active low input.
5	DE	Driver enable input. This is an active high input
6	D	Driver transmit data input.
7	GND ₁	Ground 1, the ground reference for Isolator Side 1
8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	GND ₂	Ground 2, the ground reference for Isolator Side 2
11	Y	Noninverting Driver Output. When the driver is disabled, or when VDD ₁ or VDD ₂ is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
12	Z	Inverting Driver Output. When the driver is disabled, or when VDD ₁ or VDD ₂ is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Receiver Input.
14	A	Noninverting Receiver Input.
15	GND ₂	Ground 2, the ground reference for Isolator Side 2
16	VDD ₂	Power Supply for Isolator Side 2

7.0 ORDER INFORMATION

Part No.	Isolation Rating(kV _{RMS})	Duplex	Max Data Rate (MHz)	Temperature	No. of Nodes	Package
NSi83085	5	Half	0.5	-40 to 85°C	256	WB SOIC16
NSi83086	5	Full	16	-40 to 85°C	256	WB SOIC16

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ° C according to the JEDEC industry standard classifications and peak solder temperatures.

8.0 REVISION HISTORY

Revision	Description	Date
1.0		2018/7/15
1.2	Add NSi83086 spec	2018/10/15
1.3	Change table 3.1 VDE insulation Characteristics	2018/12/20